

# HEF4052B

## Dual 4-channel analog multiplexer/demultiplexer

Rev. 11 — 15 December 2021

Product data sheet

## 1. General description

The HEF4052B is a dual single-pole quad-throw analog switch (2x SP4T) suitable for use in analog or digital 4:1 multiplexer/demultiplexer applications. Each switch features four independent inputs/outputs (nY0, nY1, nY2 and nY3) and a common input/output (nZ). A digital enable input (E) and two digital select inputs (S1 and S2) are common to both switches. When E is HIGH, the switches are turned off. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{DD}$ .

## 2. Features and benefits

- Wide supply voltage range from 3.0 V to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Complies with JEDEC standard JESD 13-B
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-B exceeds 200 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

## 3. Applications

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

## 4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
HEF4052BT	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
HEF4052BTT	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

### 5. Functional diagram

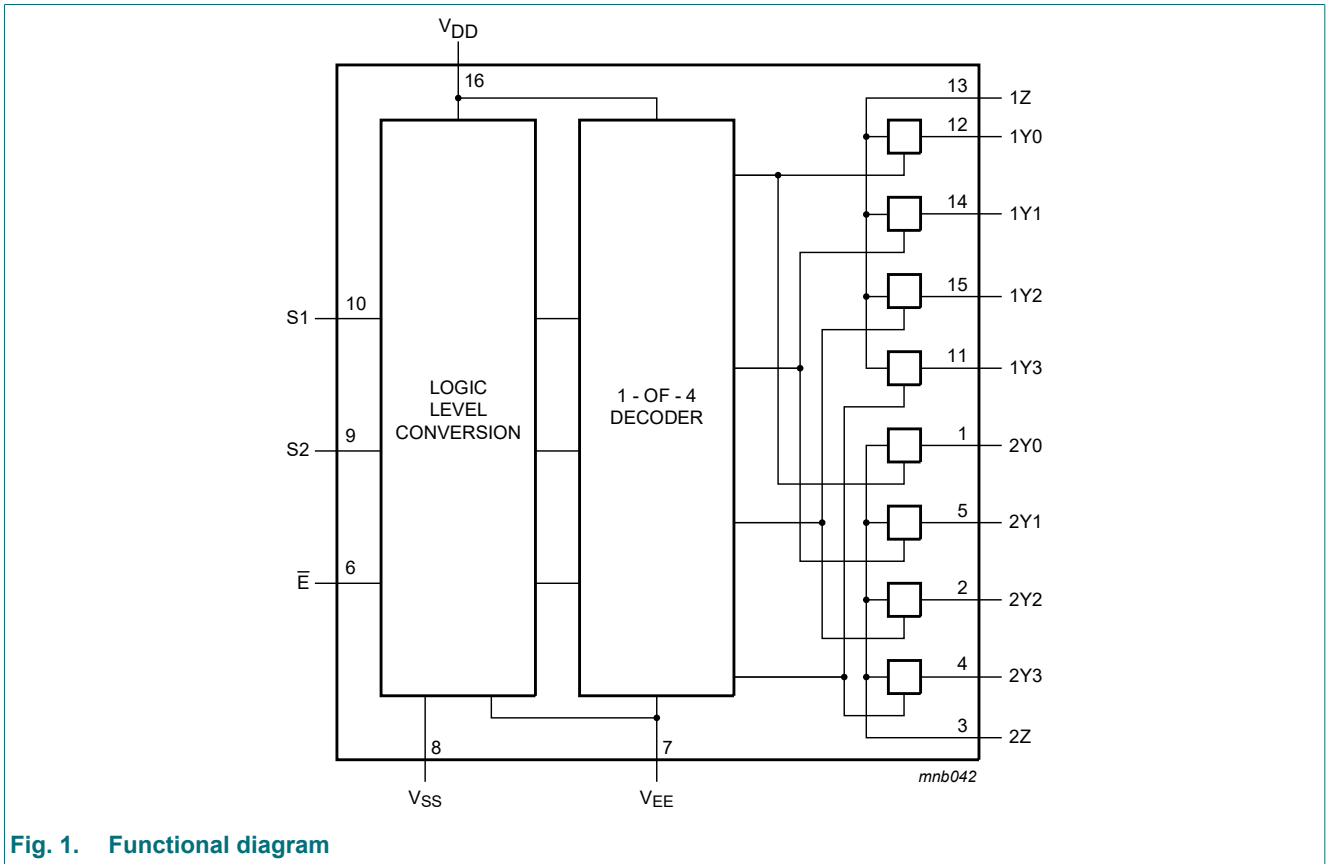


Fig. 1. Functional diagram

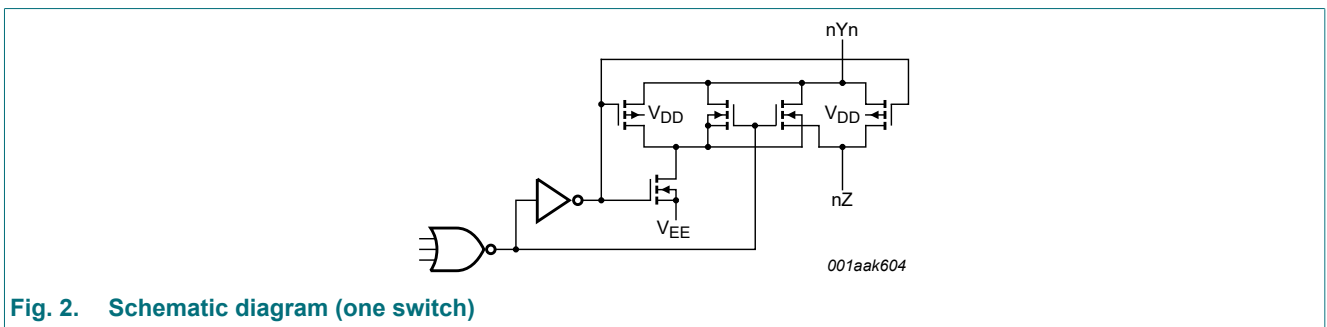


Fig. 2. Schematic diagram (one switch)

Dual 4-channel analog multiplexer/demultiplexer

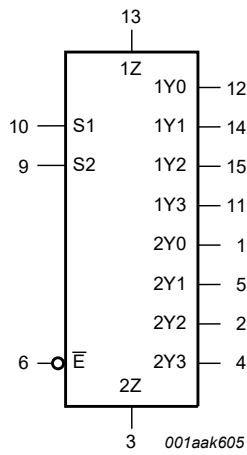


Fig. 3. Logic symbol

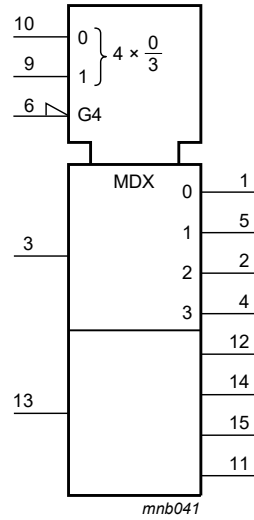


Fig. 4. IEC logic symbol

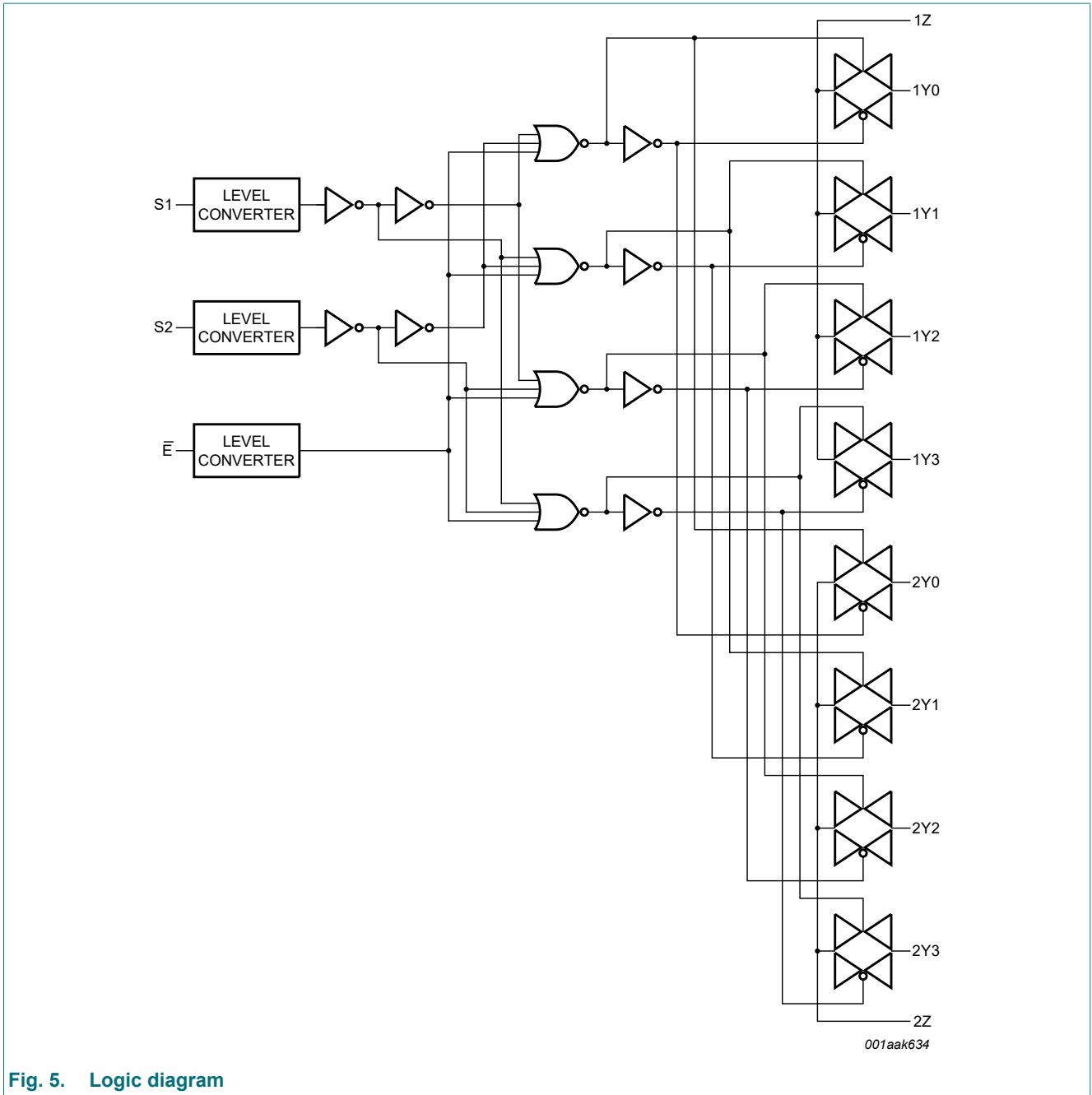


Fig. 5. Logic diagram

## 6. Pinning information

### 6.1. Pinning

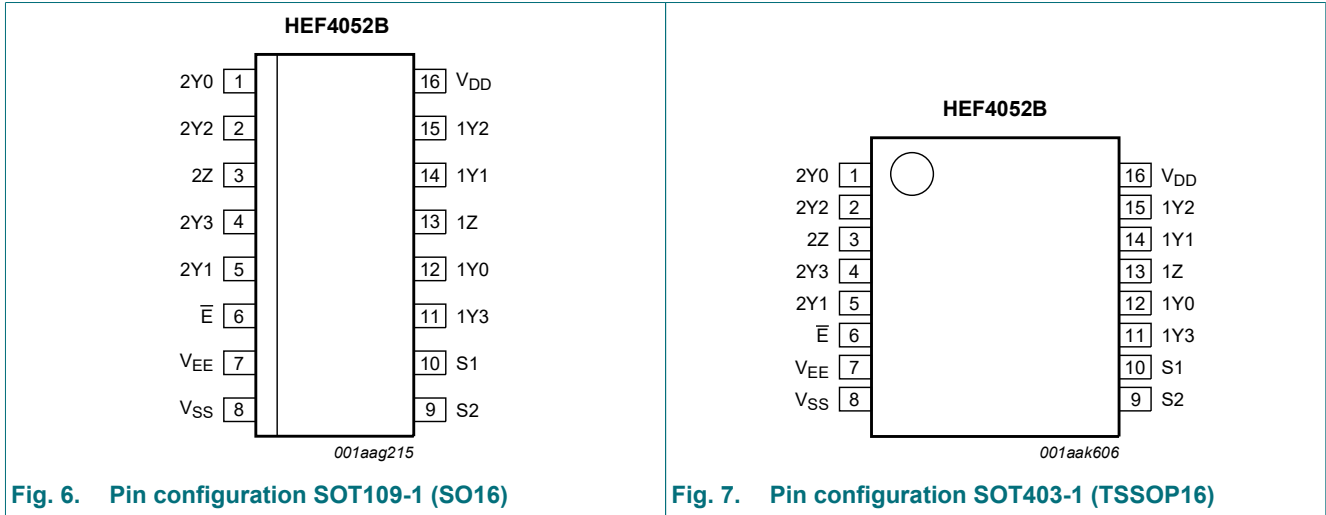


Fig. 6. Pin configuration SOT109-1 (SO16)

Fig. 7. Pin configuration SOT403-1 (TSSOP16)

### 6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$\bar{E}$	6	enable input (active LOW)
$V_{EE}$	7	supply voltage
$V_{SS}$	8	ground supply voltage
S1, S2	10, 9	select input
1Y0, 1Y1, 1Y2, 1Y3, 2Y0, 2Y1, 2Y2, 2Y3	12, 14, 15, 11, 1, 5, 2, 4	independent input or output
1Z, 2Z	13, 3	common output or input
$V_{DD}$	16	supply voltage

## 7. Function table

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input			Channel on
$\bar{E}$	S2	S1	
L	L	L	nY0 to nZ
L	L	H	nY1 to nZ
L	H	L	nY2 to nZ
L	H	H	nY3 to nZ
H	X	X	switches off

## 8. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to  $V_{SS} = 0\text{ V}$  (ground).

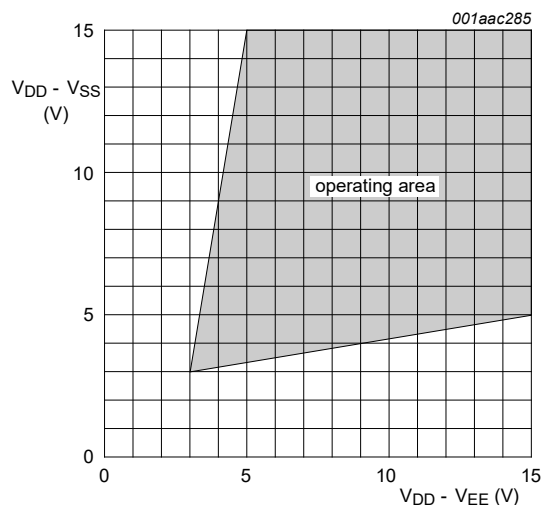
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		-0.5	+18	V
$V_{EE}$	supply voltage	referenced to $V_{DD}$ [1]	-18	+0.5	V
$I_{IK}$	input clamping current	pins Sn and E; $V_I < -0.5\text{ V}$ , or $V_I > V_{DD} + 0.5\text{ V}$	-	$\pm 10$	mA
$V_I$	input voltage		-0.5	$V_{DD} + 0.5$	V
$I_{I/O}$	input/output current		-	$\pm 10$	mA
$I_{DD}$	supply current		-	50	mA
$T_{stg}$	storage temperature		-65	+150	°C
$T_{amb}$	ambient temperature		-40	+125	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ [2]	-	500	mW
$P$	power dissipation	per output	-	100	mW

- [1] To avoid drawing  $V_{DD}$  current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no  $V_{DD}$  current will flow out of terminals Y, and in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed  $V_{DD}$  or  $V_{EE}$ .
- [2] For SOT109-1 (SO16) package:  $P_{tot}$  derates linearly with 12.4 mW/K above 110 °C.  
For SOT403-1 (TSSOP16) package:  $P_{tot}$  derates linearly with 8.5 mW/K above 91 °C.

## 9. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD}$	supply voltage	see Fig. 8	3	-	15	V
$V_I$	input voltage		0	-	$V_{DD}$	V
$T_{amb}$	ambient temperature	in free air	-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5\text{ V}$	-	-	3.75	$\mu\text{s/V}$
		$V_{DD} = 10\text{ V}$	-	-	0.5	$\mu\text{s/V}$
		$V_{DD} = 15\text{ V}$	-	-	0.08	$\mu\text{s/V}$



**Fig. 8. Operating area as a function of the supply voltages**

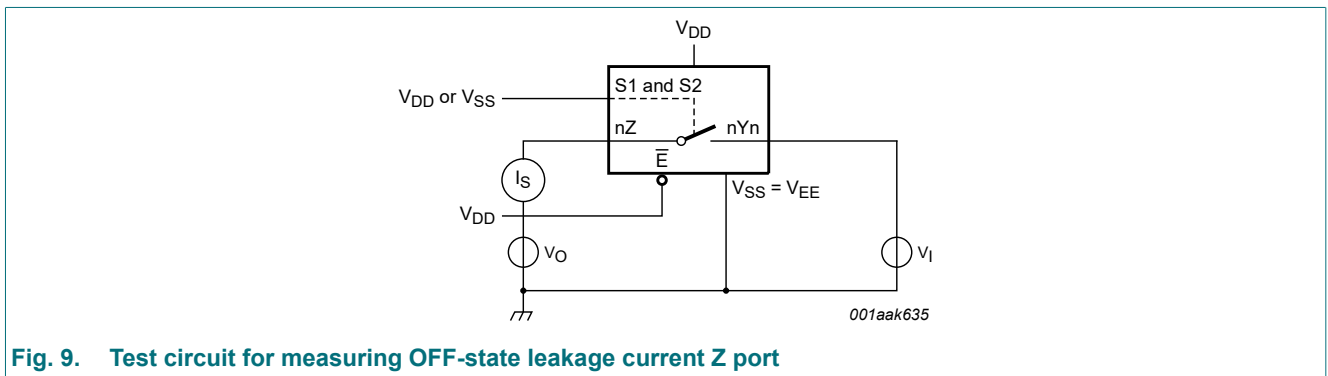
### 10. Static characteristics

**Table 6. Static characteristics**

$V_{SS} = V_{EE} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$ , unless otherwise specified.

Symbol	Parameter	Conditions	V <sub>DD</sub>	T <sub>amb</sub> = -40 °C		T <sub>amb</sub> = +25 °C		T <sub>amb</sub> = +85 °C		T <sub>amb</sub> = +125 °C		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	I <sub>O</sub>   < 1 μA	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V
V <sub>IL</sub>	LOW-level input voltage	I <sub>O</sub>   < 1 μA	5 V	-	1.5	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	-	4.0	V
I <sub>I</sub>	input leakage current		15 V	-	±0.1	-	±0.1	-	±1.0	-	±1.0	μA
I <sub>S(OFF)</sub>	OFF-state leakage current	Z port; all channels OFF; see Fig. 9	15 V	-	-	-	1000	-	-	-	-	nA
		Y port; per channel; see Fig. 10	15 V	-	-	-	200	-	-	-	-	nA
I <sub>DD</sub>	supply current	I <sub>O</sub> = 0 A	5 V	-	5	-	5	-	150	-	150	μA
			10 V	-	10	-	10	-	300	-	300	μA
			15 V	-	20	-	20	-	600	-	600	μA
C <sub>I</sub>	input capacitance	Sn, $\bar{E}$ inputs	-	-	-	-	7.5	-	-	-	-	pF

#### 10.1. Test circuits



**Fig. 9. Test circuit for measuring OFF-state leakage current Z port**

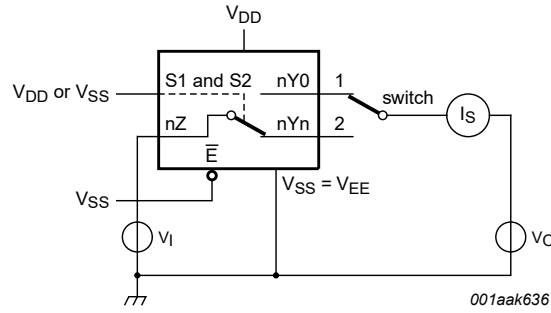


Fig. 10. Test circuit for measuring OFF-state leakage current nYn port

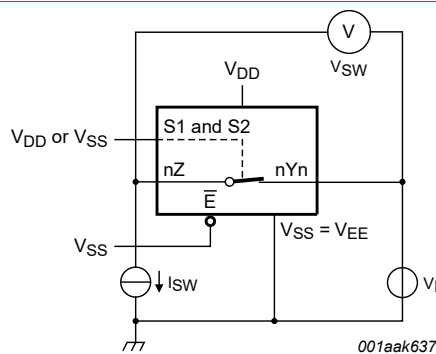
### 10.2. On resistance

Table 7. ON resistance

$T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $I_{SW} = 200\text{ }\mu\text{A}$ ;  $V_{SS} = V_{EE} = 0\text{ V}$ .

Symbol	Parameter	Conditions	$V_{DD} - V_{EE}$	Typ	Max	Unit
$R_{ON(peak)}$	ON resistance (peak)	$V_I = 0\text{ V to }V_{DD} - V_{EE}$ ; see Fig. 11 and Fig. 12	5 V	350	2500	$\Omega$
			10 V	80	245	$\Omega$
			15 V	60	175	$\Omega$
$R_{ON(rail)}$	ON resistance (rail)	$V_I = 0\text{ V}$ ; see Fig. 11 and Fig. 12	5 V	115	340	$\Omega$
			10 V	50	160	$\Omega$
			15 V	40	115	$\Omega$
		$V_I = V_{DD} - V_{EE}$ ; see Fig. 11 and Fig. 12	5 V	120	365	$\Omega$
			10 V	65	200	$\Omega$
			15 V	50	155	$\Omega$
$\Delta R_{ON}$	ON resistance mismatch between channels	$V_I = 0\text{ V to }V_{DD} - V_{EE}$ ; see Fig. 11	5 V	25	-	$\Omega$
			10 V	10	-	$\Omega$
			15 V	5	-	$\Omega$

#### 10.2.1. On resistance waveform and test circuit



$$R_{ON} = V_{SW} / I_{SW}$$

Fig. 11. Test circuit for measuring  $R_{ON}$

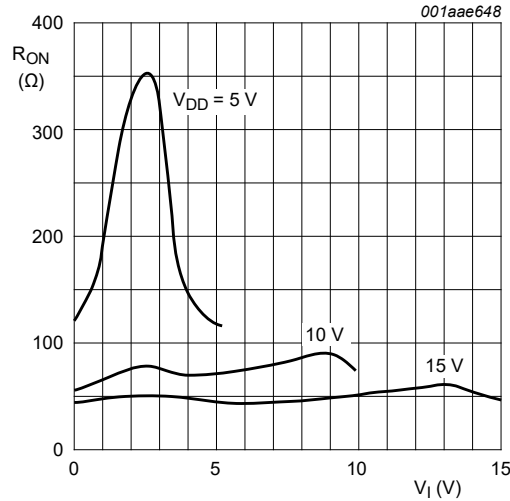


Fig. 12. Typical  $R_{ON}$  as a function of input voltage

## 11. Dynamic characteristics

Table 8. Dynamic characteristics

$T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $V_{SS} = V_{EE} = 0\text{ V}$ ; for test circuit see Fig. 16.

Symbol	Parameter	Conditions	$V_{DD}$	Typ	Max	Unit
$t_{PHL}$	HIGH to LOW propagation delay	nYn, nZ to nZ, nYn; see Fig. 13	5 V	10	20	ns
			10 V	5	10	ns
			15 V	5	10	ns
		Sn to nYn, nZ; see Fig. 14	5 V	150	305	ns
			10 V	65	135	ns
			15 V	50	100	ns
$t_{PLH}$	LOW to HIGH propagation delay	Yn, nZ to nZ, nYn; see Fig. 13	5 V	10	20	ns
			10 V	5	10	ns
			15 V	5	10	ns
		Sn to nYn, nZ; see Fig. 14	5 V	150	300	ns
			10 V	75	150	ns
			15 V	50	100	ns
$t_{PHZ}$	HIGH to OFF-state propagation delay	$\bar{E}$ to nYn, nZ; see Fig. 15	5 V	95	190	ns
			10 V	90	180	ns
			15 V	85	180	ns
$t_{PZH}$	OFF-state to HIGH propagation delay	$\bar{E}$ to nYn, nZ; see Fig. 15	5 V	130	260	ns
			10 V	55	115	ns
			15 V	45	85	ns
$t_{PLZ}$	LOW to OFF-state propagation delay	$\bar{E}$ to nYn, nZ; see Fig. 15	5 V	100	205	ns
			10 V	90	180	ns
			15 V	90	180	ns
$t_{PZL}$	OFF-state to LOW propagation delay	$\bar{E}$ to nYn, nZ; see Fig. 15	5 V	120	240	ns
			10 V	50	100	ns
			15 V	35	75	ns

11.1. Waveforms and test circuit

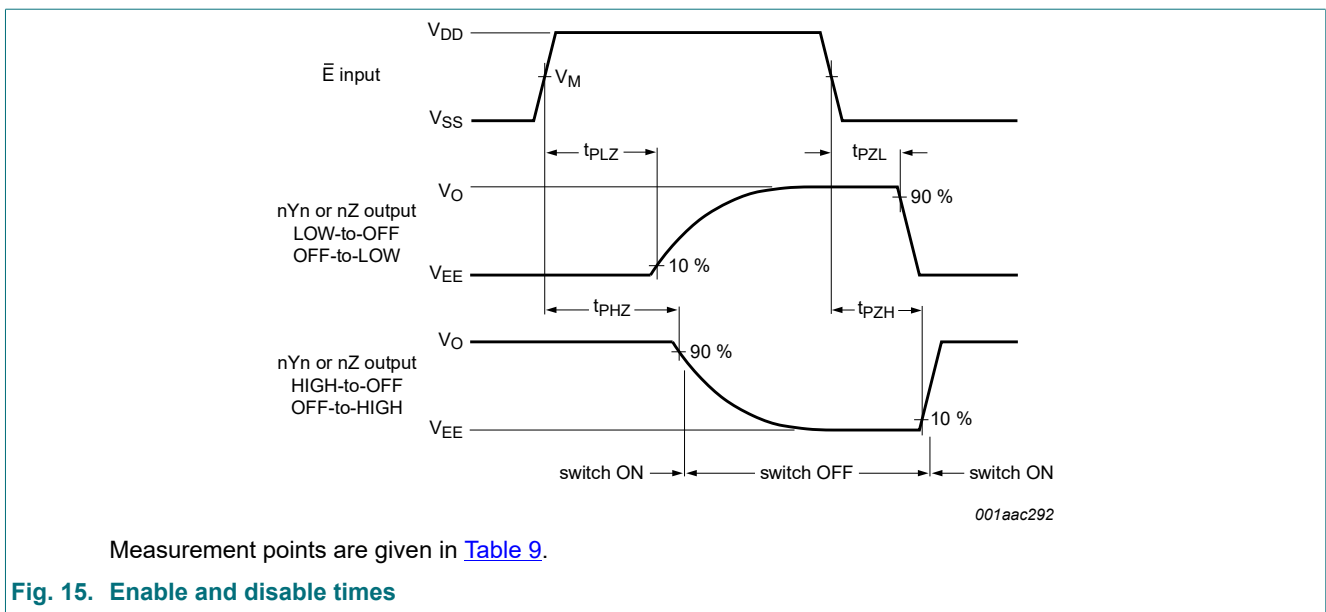
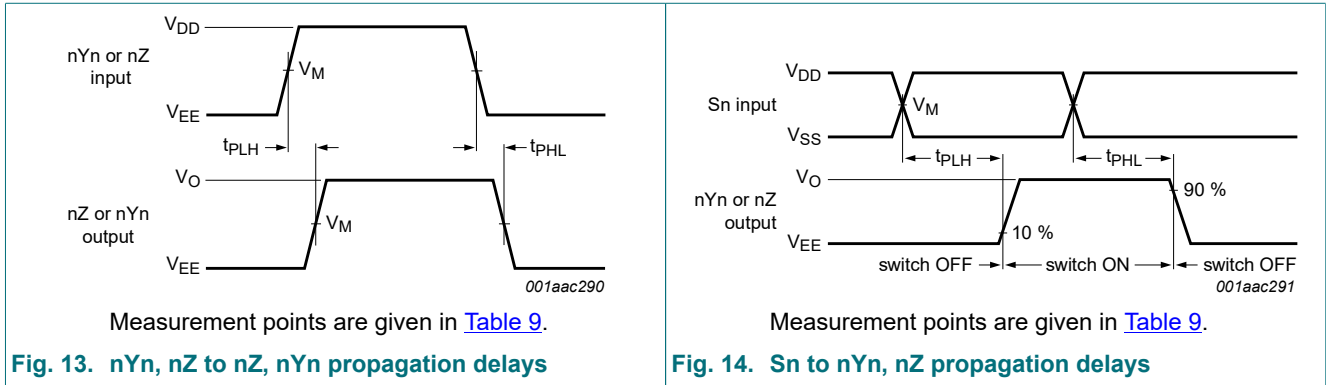
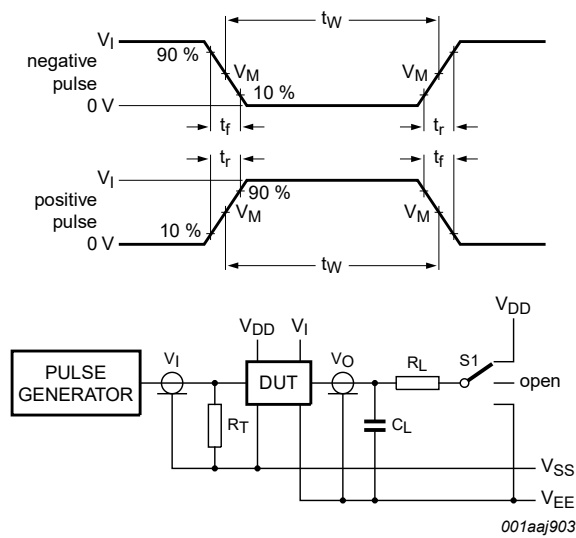


Table 9. Measurement points

Supply voltage	Input	Output
$V_{DD}$	$V_M$	$V_M$
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$



Test data is given in [Table 10](#).

Definitions:

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator;

$C_L$  = Load capacitance including test jig and probe;

$R_L$  = Load resistance.

**Fig. 16. Test circuit for measuring switching times**

**Table 10. Test data**

Input				Load		S1 position				
nYn, nZ	Sn and $\bar{E}$	$t_r, t_f$	$V_M$	$C_L$	$R_L$	$t_{PHL}$ [1]	$t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$	other
$V_{DD}$ or $V_{EE}$	$V_{DD}$ or $V_{SS}$	$\leq 20$ ns	$0.5V_{DD}$	50 pF	10 k $\Omega$	$V_{DD}$ or $V_{EE}$	$V_{EE}$	$V_{EE}$	$V_{DD}$	$V_{EE}$

[1] For nYn to nZ propagation delays use  $V_{EE}$ . For Sn to nYn or nZ propagation delays use  $V_{DD}$ .

## 11.2. Additional dynamic parameters

**Table 11. Additional dynamic characteristics**

$V_{SS} = V_{EE} = 0$  V;  $T_{amb} = 25$  °C.

Symbol	Parameter	Conditions	$V_{DD}$	Typ	Max	Unit
THD	total harmonic distortion	see <a href="#">Fig. 17</a> ; $R_L = 10$ k $\Omega$ ; $C_L = 15$ pF; channel ON; $V_I = 0.5V_{DD}$ (p-p); $f_i = 1$ kHz	[1] 5 V	0.25	-	%
			10 V	0.04	-	%
			15 V	0.04	-	%
$f_{(-3dB)}$	-3 dB frequency response	see <a href="#">Fig. 18</a> ; $R_L = 1$ k $\Omega$ ; $C_L = 5$ pF; channel ON; $V_I = 0.5V_{DD}$ (p-p)	[1] 5 V	13	-	MHz
			10 V	40	-	MHz
			15 V	70	-	MHz
$\alpha_{iso}$	isolation (OFF-state)	see <a href="#">Fig. 19</a> ; $f_i = 1$ MHz; $R_L = 1$ k $\Omega$ ; $C_L = 5$ pF; channel OFF; $V_I = 0.5V_{DD}$ (p-p)	[1] 10 V	-50	-	dB
$V_{ct}$	crosstalk voltage	digital inputs to switch; see <a href="#">Fig. 20</a> ; $R_L = 10$ k $\Omega$ ; $C_L = 15$ pF; $\bar{E}$ or Sn = $V_{DD}$ (square-wave)	10 V	50	-	mV
Xtalk	crosstalk	between switches; see <a href="#">Fig. 21</a> ; $f_i = 1$ MHz; $R_L = 1$ k $\Omega$ ; $V_I = 0.5V_{DD}$ (p-p)	[1] 10 V	-50	-	dB

[1]  $f_i$  is biased at  $0.5 V_{DD}$ ;  $V_I = 0.5V_{DD}$  (p-p).

Table 12. Dynamic power dissipation

$P_D$  can be calculated from the formulas shown;  $V_{EE} = V_{SS} = 0\text{ V}$ ;  $t_r = t_f \leq 20\text{ ns}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ .

Symbol	Parameter	$V_{DD}$	Typical formula for $P_D$ ( $\mu\text{W}$ )	where:
$P_D$	dynamic power dissipation	5 V	$P_D = 1300 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$f_i$ = input frequency in MHz; $f_o$ = output frequency in MHz; $C_L$ = output load capacitance in pF; $V_{DD}$ = supply voltage in V; $\Sigma(C_L \times f_o)$ = sum of the outputs.
		10 V	$P_D = 6100 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	
		15 V	$P_D = 15600 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	

11.2.1. Test circuits

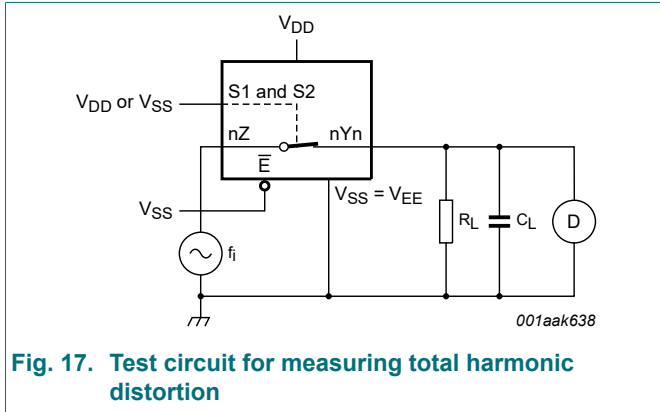


Fig. 17. Test circuit for measuring total harmonic distortion

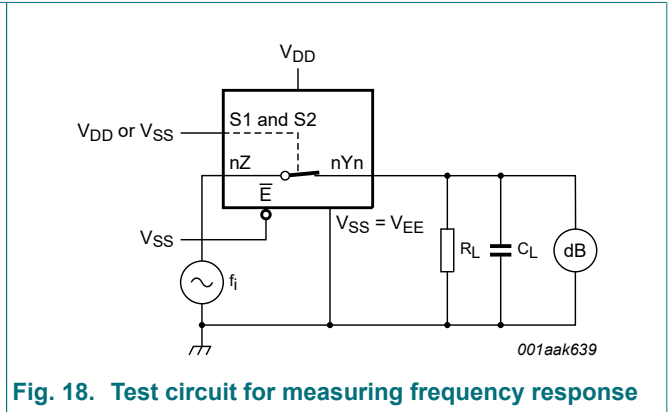


Fig. 18. Test circuit for measuring frequency response

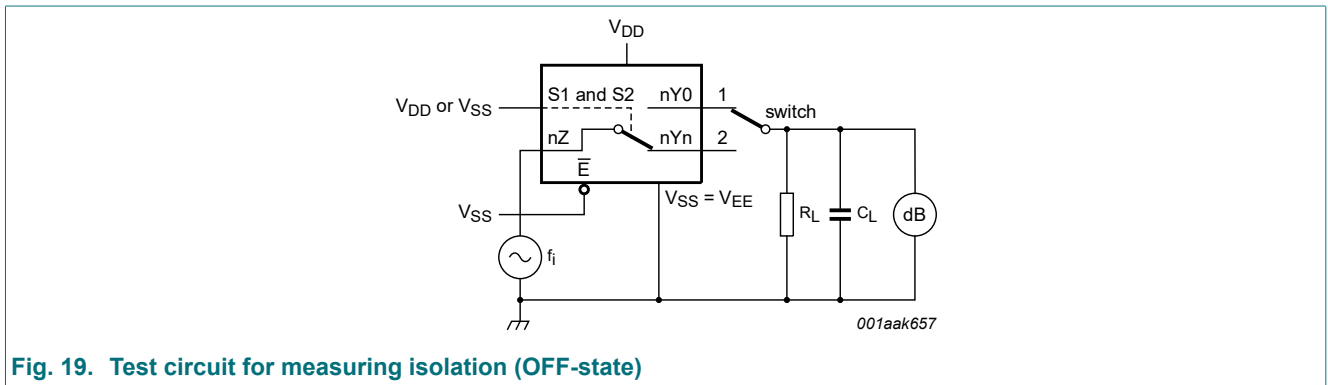
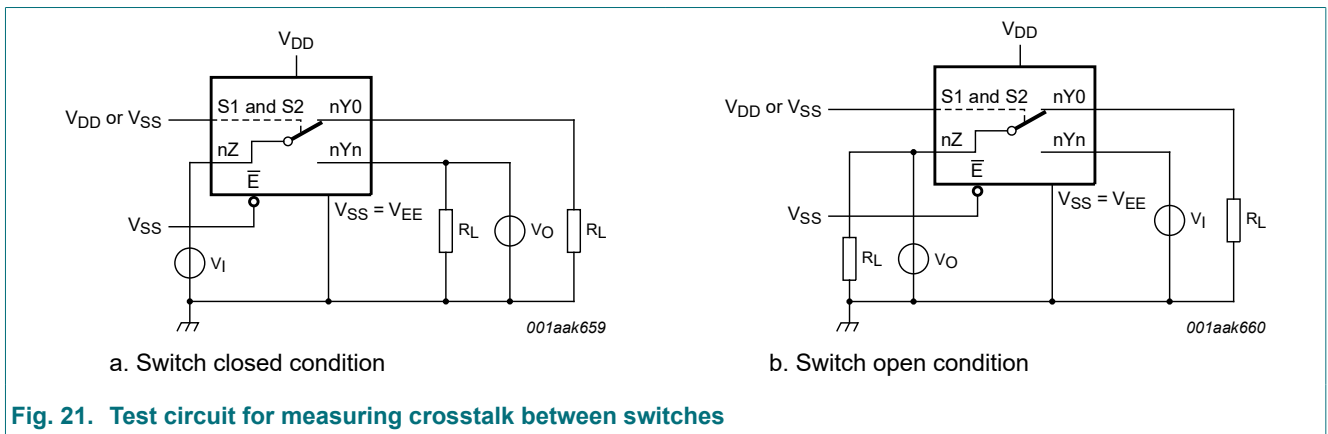
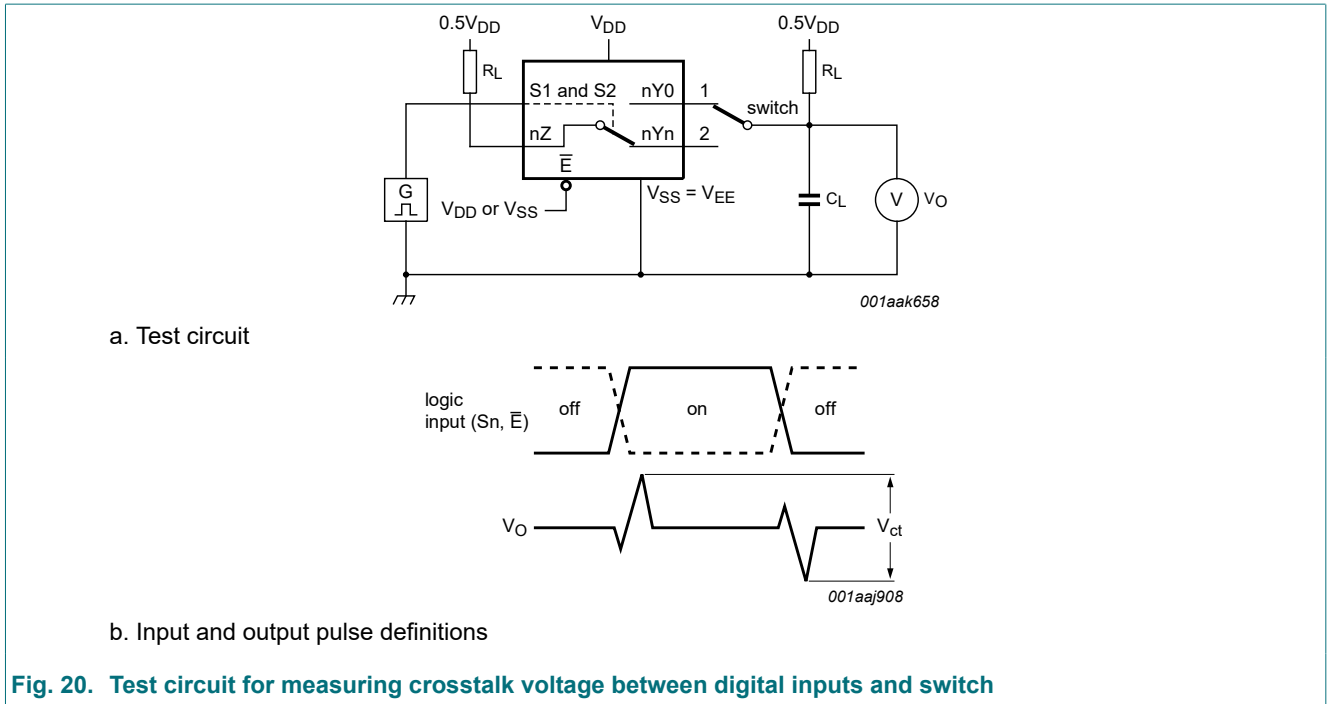


Fig. 19. Test circuit for measuring isolation (OFF-state)



12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

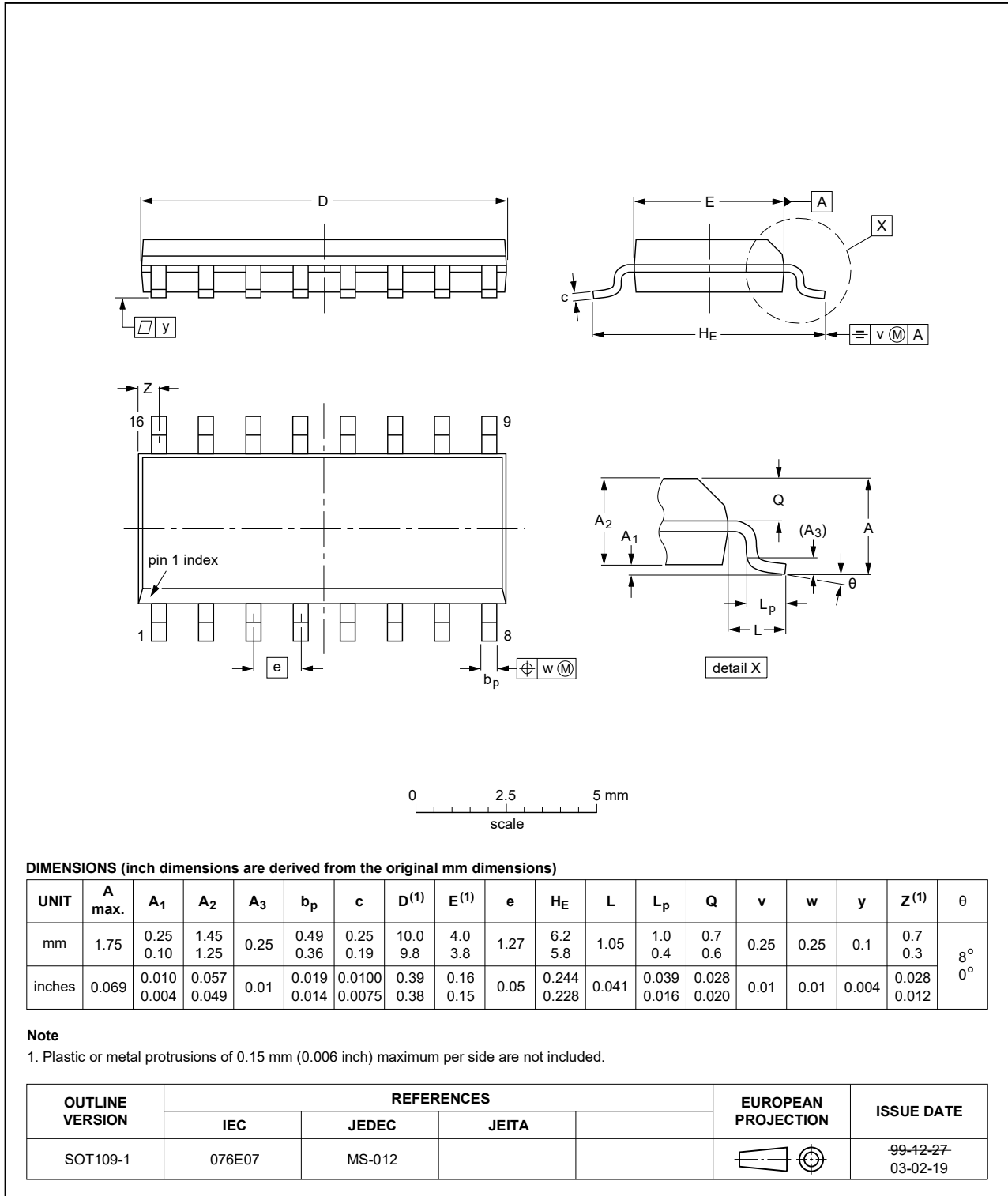


Fig. 22. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

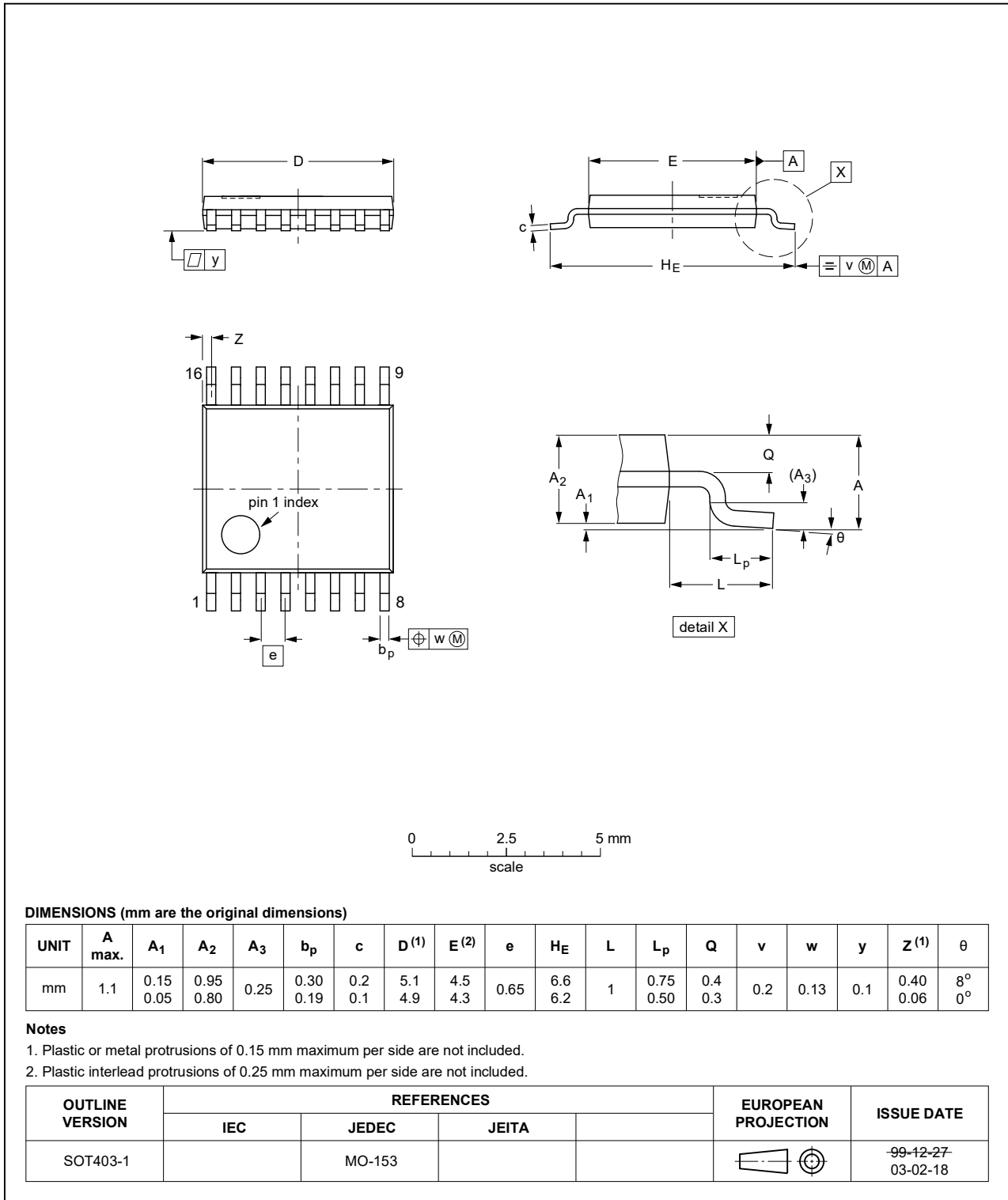


Fig. 23. Package outline SOT403-1 (TSSOP16)

## 13. Abbreviations

Table 13. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

## 14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4052B v.11	20211215	Product data sheet	-	HEF4052B v.10
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> <li><a href="#">Table 4</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> <li><a href="#">Table 13</a> updated.</li> </ul>			
HEF4052B v.10	20160325	Product data sheet	-	HEF4052B v.9
Modifications:	<ul style="list-style-type: none"> <li>Type number HEF4052BP (SOT38-4) removed.</li> </ul>			
HEF4052B v.9	20140911	Product data sheet	-	HEF4052B v.8
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Fig. 20</a>: Test circuit modified</li> </ul>			
HEF4052B v.8	20111117	Product data sheet	-	HEF4052B v.7
Modifications:	<ul style="list-style-type: none"> <li>Legal pages updated.</li> <li>Changes in <a href="#">Section 1</a>, <a href="#">Section 2</a>, and <a href="#">Section 3</a>.</li> </ul>			
HEF4052B v.7	20100326	Product data sheet	-	HEF4052B v.6
HEF4052B v.6	20100308	Product data sheet	-	HEF4052B v.5
HEF4052B v.5	20091127	Product data sheet	-	HEF4052B v.4
HEF4052B v.4	20090924	Product data sheet	-	HEF4052B_CNV v.3
HEF4052B_CNV v.3	19950101	Product specification	-	HEF4052B_CNV v.2
HEF4052B_CNV v.2	19950101	Product specification	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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